Guest Editorial

IN the past decade, we have seen the growing application of real-time systems principles in new areas. The wide adoption of technologies derived from the domain of real-time systems has already resulted in significant impacts on how automated systems are designed and deployed. Solutions with better intelligence and flexibility are provided at lower cost and more functionality. Another trend is on the integration of manufacturing and services. In order to remain competitive, solutions must be dynamic, configurable, and/or upgradeable. As industrial systems become more intelligent, key technologies are needed to provide distributed and collaborative industrial environments.

Real-time systems are systems that must respond to external stimuli in a timely fashion. Tasks are often associated with hard, soft, or firm deadlines in executions. The correctness of a real-time system depends on not only the logical correctness of its tasks but also the timeliness of their executions. Intelligent resource allocation technologies and rigorous analysis methodologies provide important foundation in system designs and implementations. This Special Section on "Real-Time Systems" aims at presenting some of the most significant research works representing the state-of-the-art in the area of the real-time systems for automation systems. In particular, four papers are included in this special issue.

The first paper, entitled "ORTEGA: An Efficient and Flexible Online Fault Tolerance Architecture for Real-Time Control Systems," focuses on how to tolerate software faults in real-time control systems. There are three types of software faults under consideration. A resource sharing fault occurs when the code and/or data of some module is corrupted. A timing fault occurs when the system fails to meet any timing constraint. A semantic fault occurs when some wrong value is produced. This paper improves Simplex, that is a software architecture for the design of dependable real-time control systems, with respect to its major problems in efficiency and flexibility. A new fault tolerance architecture called ORTEGA is proposed to maintain high fault coverage and reliability as the original Simplex and meanwhile significantly improves the flexibility and resource utilization efficiency. A high-assurance controller is activated only when a fault is detected. The improvement on resource utilization is important to resource-constrained real-time embedded systems. ORTEGA also allows the high-performance controller and high-assurance controller to run at different rates, that greatly facilitates in control and fault tolerance design.

The second paper, entitled "Analyzing TDMA With Slot Skipping," is on the analysis of time division multiple access (TDMA) with slot skipping. TDMA protocols aim at the resolving of the communication medium sharing problem when real-time requirements must be satisfied. Under TDMA, messages are assigned to time slots in a way that no two nodes transmit at the same time, and the queuing delays of messages are bounded. In order to meet all deadlines, it may be necessary that a message stream with periodic messages uses a specific time slot in a TDMA cycle only in a few cycles, while in the majority of the cycles that time slot is not used. This paper considers the skipping of a slot when it is not used. Hence, the next slot can start earlier in benefit of hard real-time traffic. This model is applicable to P-NET, defined in an international fieldbus standard. In this work, a schedulability analysis for TDMA networks with slot skipping is presented.

The third paper, entitled "A Hierarchical Framework for Design Space Exploration and Optimization of TTP-Based Distributed Embedded Systems," proposes an efficient design space exploring (DSE) framework for distributed embedded systems under the time-triggered protocol. The time-triggered protocol is a TDMA-based bus protocol designed for use in safety-critical avionics and automotive distributed embedded systems. A two-level hierarchical DSE framework is proposed to minimize the total bus utilization while meeting an end-to-end deadline constraint. Logic-based Benders decomposition is adopted to divide the optimization problem into a master problem (of mapping tasks to CPU nodes) and a subproblem (of finding a feasible solution of bus access configuration and task/message schedule). The approach provides clean decomposition of the optimization problem into a master problem and a subproblem, so that the master problem can be solved separately, independent from the subproblem. It helps to reduce the workload of selected problem solvers to increase efficiency and scalability. This work considers statically scheduled distributed embedded systems, where both software tasks and network messages are scheduled offline.

The fourth paper, entitled "Adaptive Multilevel Code Update Protocol for Real-Time Sensor Operating," presents a protocol for updating or adding programs on sensor nodes via communication channel at run-time. Considering that in sensor networks each node has very limited resources, and it is very hard to find and re-gather them, the proposed protocol enables energy-efficient code update by supporting multilevel code management. It adaptively selects a protocol that meets the application deadlines and consumes less energy based on the cost analysis of several protocols. Simulation results show that the proposed approach can reduce energy consumption compared with the existing single-level code update protocols while meeting the deadlines of the running applications.

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