Open Issues in the SoC Design

IES 2006

Panelists

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- Gaël CLAVE – Texas Instruments
- Jean-François DUBOC – FITechno

- Robert de SIMONE – INRIA
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IES'2006

Panel: Open Issues in SoC Design

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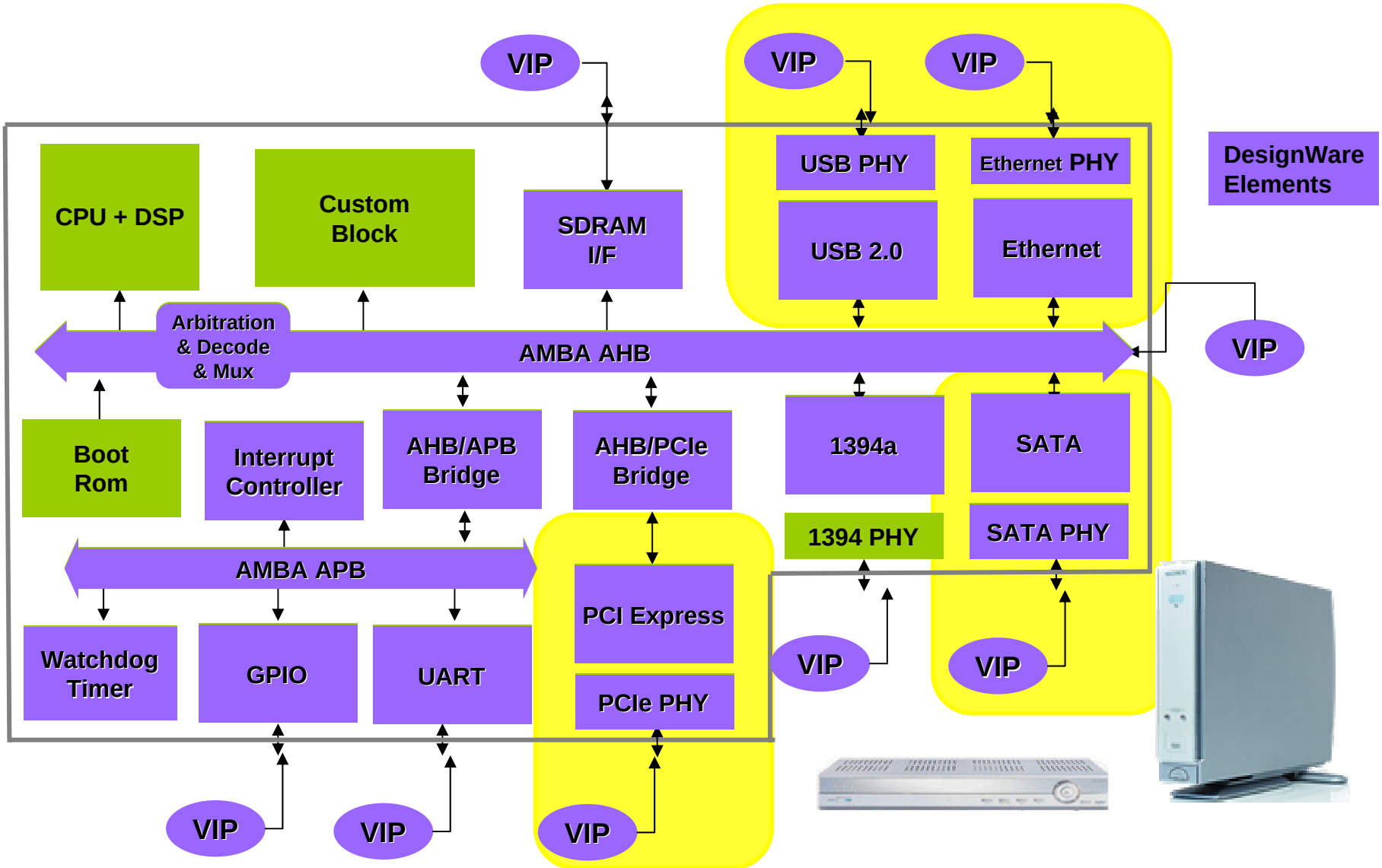
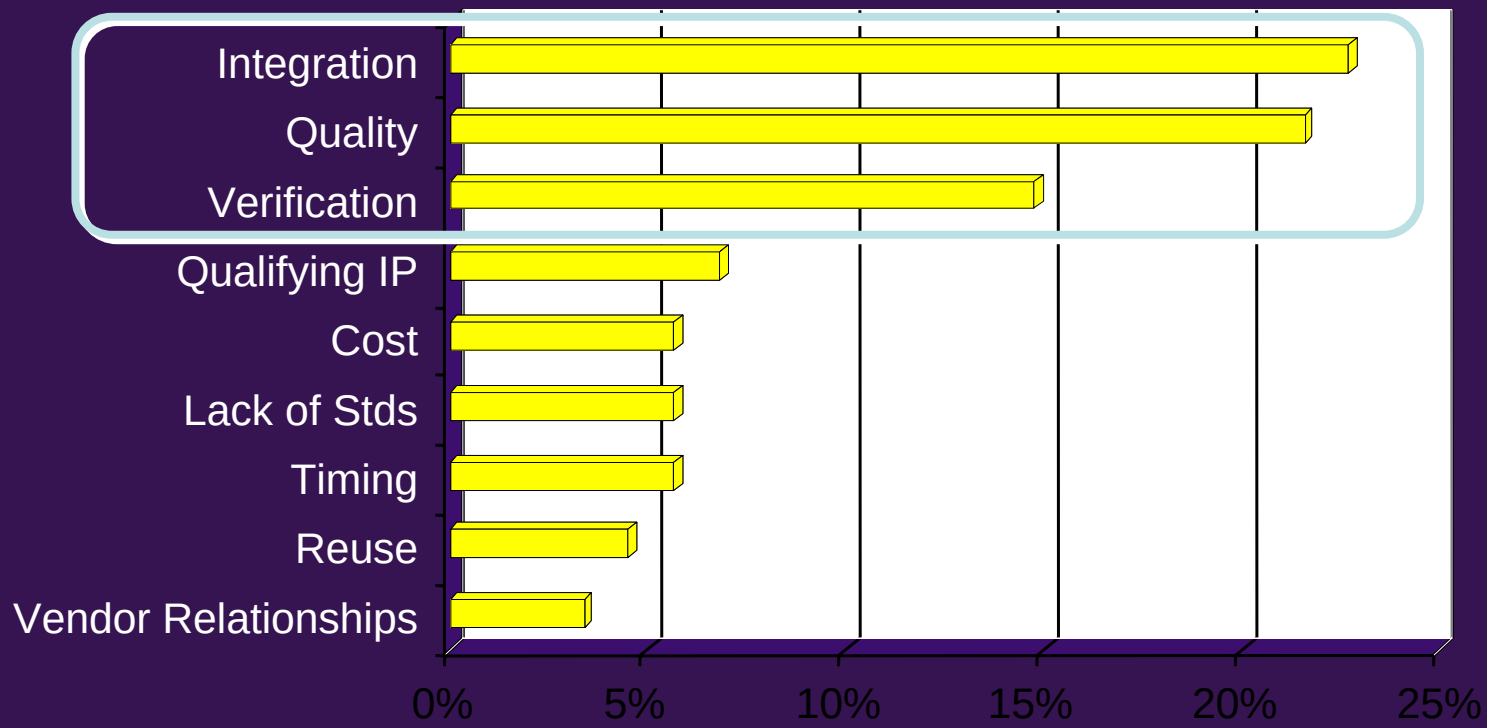
Targeted SoC – Set Top Box



Configurability is Critical & Complex

DAC Study

What is the biggest challenge for the IP User of the future?



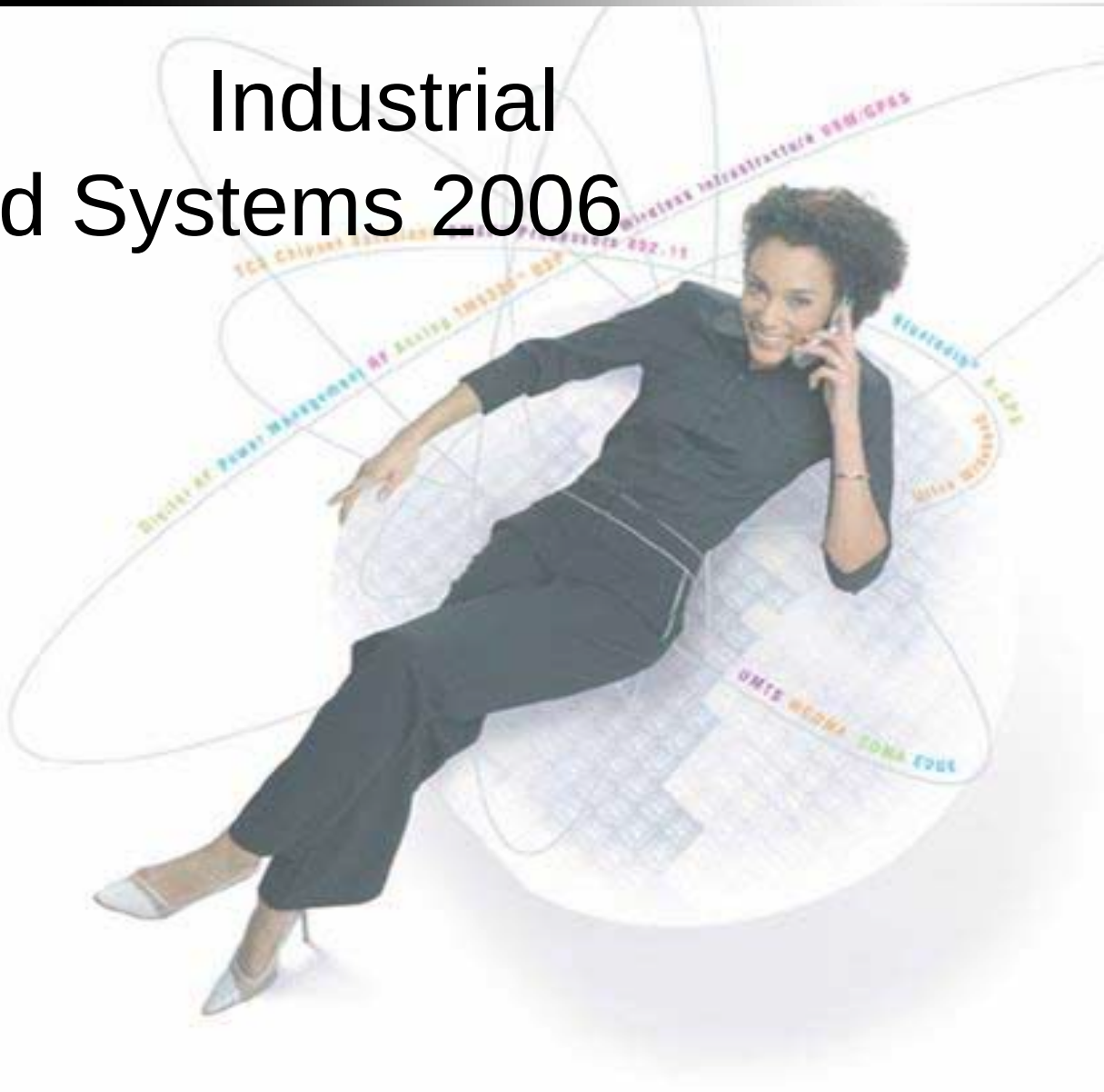
What are the solutions ?

- All Industry Successful High Volume SoC are based on Industry Standards.
  - Applications Standards (Set Top Box–DVD–Mobile Phones)
  - IP Interconnect/InterOperability (SPIRIT IP XACT)
  - IP Quality (VSIA QIP)

Issue

- Why are there so little Universities/Research Organisations Associate Members in Standard Organisations ?
  - VSIA
    - CNRS Brazil , STARC
  - SPIRIT
    - STARC

Industrial Embedded Systems 2006



IES-06 : New Challenges for SoC

- The new SoC generation shows a very large content of embedded Sw with OS's, Multimedia codes, Crypto's, Modem's , Software Define Radio , Power Management, which are supported by more and more complex platforms.

- A convergence between Hw and Sw communities creates new needs in term of input formalism and specifications.
- The ever growing SW sizes and multicores platforms are asking for advance modeling technologies and ultra high speed simulator.
- Time to Market to implement new standards or upgrade features pave the way for Behavioral Synthesis.
- Verification as usual is the bottleneck.

IES-06 : New Challenges for SoC

Input formalism and specifications:

Beyond fashions, the reality is a deep disconnect between Sw and Hw development methodologies and languages.

The Java wave is gone away for SW, the ubiquitous SystemC is there for HW….modeling.

Most of used SW code running on a SoC platform are written in C or C++ .

All Hw is described using HDL Vhdl/Verilog. This Hw may be either non programmable and only need parameterization sequences as DMA caches… or programmable/reconfigurable/networked as Cpu arrays within a NoC.

How to federate these needs in a common framework?

How to bridge?

How to partition Sw's between Cpu's and wired FU's

IES-06 : New Challenges for SoC

Modeling and simulation:

A simple link setup when a telephone is powered up may take 10sec with 2 Cpu cores running at 250Mhz plus massive Hw accelerator.

Sw simulation speed requirement for a full SoC platform is now in the range of 10 to 100Mips/per core with more demand on cycle accuracy.

Early architecture tradeoff to handle all system uses-cases and grant performances push the modeling effort up front a SoC development.

Which formalism allows very early architecture description with SystemC/RTL co-generation?

How to spin off easily a Cpu ISS, regenerate its tool kit and refresh the SoC model?

IES-06 : New Challenges for SoC

Implementing Sw standards:

- The multimedia Sw requirement in wireless application force SoC developers to off load regular Cpu cores in dedicated Hw or dedicated cores.

- Behavioral Synthesis technologies have now reach an industrial quality and challenge handcrafted Hw to implement C based data flow in wired Hw.
- Routing the data through the SoC is always the most power consuming task

- How to partition Sw in multicore environment and reconfigurable data routing?

Low Power and design Reuse

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Reusability background

- Design Reuse is 10 years old
- It appears with the general usage of embedded processors and standard interfaces
- It generates rules like synchronous design, bi-directional busses ….
- It was the way to
  - Keep control of project schedule while complexity increase
  - Minimize risk
  - Control development cost

How was handle low power?

- For technologies above 90 nm, leakage currents were negligible
- Goal was to stop the clock in a block or sub part of system when this part was not used
- Gated clock strategy driven by software
- Automatic detection by hardware in processor cores
  - Instruction decoding in pipeline allows to enable the clock in the units which are used by instruction execution
- Register controlled by embedded processor
  - Writing to a bit in a register enables or disable the clock in the block
- No limitations for Design Reuse of IPs

What has changed

- Below 90 nm, leakage currents have the same magnitude than current than dynamic current when a block is used
- Stopping the clock is not enough
- Power supply has to be cut to really avoid leakage current
- Requires physical isolation
- How to handle context saving

Power isolation

- When the power is cut in a block, its I/O can discharge the transistors in the neighborhood
- The bloc has to be physically decoupled by the usage of level shifters on each I/O
- Challenge:
  - In each system, the isolation of an IP can be different (used alone in one device, with other blocks in an other one)
  - Level Shifters are analogue cells and the back end design becomes mixed signal back end design, increasing complexity and issues

Context Saving

- If a block has to be initialized before any usage, there is no issue
- Between two burst mode, a GSM chip has no activity but has to restart very quickly on regular basis:
  - Complete reset not acceptable
  - Keep power all the time is not acceptable
- Methodology:
  - Keep power in some parts of the registers to save the context
  - Transfer thru serial link context to an always power on part of the design and restore in the same way

Conclusion

- Power isolation is system specific and will impact any IP on each usage
- Context saving will depend of the block, the system where it is used, various modes of the system ….
- IP and Design Reuse are less easy than before
- Work to be done for any IP reuse across various designs